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January 5, 2004

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/697,520 10/30/03

Seiki Ogura et al.

TWIN NAND DEVICE STRUCTURE, ARRAY OPERATION AND ITS FABRICATION METHOD

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 27, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date SBA 1/27/04

Information in this Information Disclosure Statement was cited in a communication from a foreign Patent Office in a counterpart foreign application. The concise explanation of relevance for the non-English documents is provided therein. A copy of that communication is attached.

Y. Hayashi et al., "Non-volatile Semiconductor Memory and Its Programming Method," JP 11-22940, 12/05/1997, discusses how the ONO layer sandwich stores electron or whole charges in the nitride or interface trap sites.

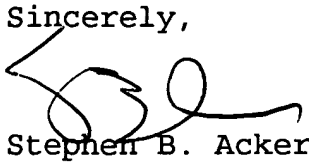
I. Fujiwara, "Non-volatile Semiconductor Memory and its Read Method," JP 2000-31435, 7/8/1998.

F. Masuoka and R. Shirota et al., "A New NAND Cell for Ultra High Density 5V-Only EEPROMS," May 1988, Proc. 1988 Symp. on VLSI Tech., IV-5, pp. 33-34, describes a floating gate NAND cell that has been used widely as Non-volatile memory.

U.S. Patent 4,943,943 to Hayashi et al., "Read-Out Circuit for Semiconductor Nonvolatile Memory," describes a read-out circuit for a semiconductor nonvolatile memory which is capable of extracting a widely fluctuating output voltage using a reverse read.

U.S. Patent 5,768,192 to Eitan, "Non-Volatile Semi-Conductor Memory Cell Utilizing Asymmetrical Charge Trapping," discloses a non-volatile semiconductor memory cell utilizing asymmetrical charge trapping.

Sincerely,



Stephen B. Ackerman, Reg. #37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
HALO-01-0140	10/697,520
Applicant: Seiki Ogura et al.	
Filing Date: 10/30/03	Group Art Unit

U.S. PATENT AND TRADEMARK OFFICE JAN 29 2004

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4943943	7/24/90	Hayashi et al.	365	185	7/24/84
	5768192	6/16/98	Eitan	365	185.24	7/23/96

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
JP	11-229400	8/5/97	Japan	H01L	27/115		
JP	00-314355	7/8/98	Japan	H01L	27/115		

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

F. Masuoka et al., "A New NAND Cell for Ultra High Density 5V-Only EEPROMs," May 1988, Proc. 1988 Symp. on VLSI Tech., IV-5, pp. 33-34.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.